

May 1997

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

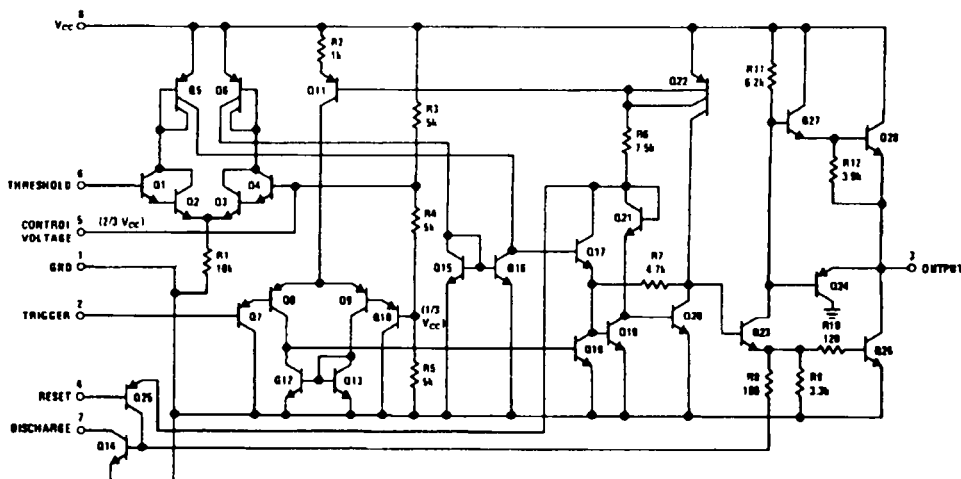
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8 pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



D6007851 1

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555H, LM555CH	760 mW
LM555, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	-55°C to +125°C

Storage Temperature Range -65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to +15V, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	$V_{CC} = 5\text{V}$, $R_L = \infty$ $V_{CC} = 15\text{V}$, $R_L = \infty$ (Low State) (Note 4)		3 10	5 12		3 10	6 15	 mA mA
Timing Error, Monostable								
Initial Accuracy	$R_A = 1\text{k}$ to $100\text{k}\Omega$, $C = 0.1\ \mu\text{F}$, (Note 5)		0.5			1		%
Drift with Temperature			30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy	$R_A, R_B = 1\text{k}$ to $100\text{k}\Omega$, $C = 0.1\ \mu\text{F}$, (Note 5)		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		$\times V_{CC}$
Trigger Voltage	$V_{CC} = 15\text{V}$	4.8	5	5.2		5		V
	$V_{CC} = 5\text{V}$	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	$V_{CC} = 15\text{V}$	9.6	10	10.4	9	10	11	V
	$V_{CC} = 5\text{V}$	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 7)								
Output Low	$V_{CC} = 15\text{V}$, $I_T = 15\text{mA}$		150			180		mV
Output Low	$V_{CC} = 4.5\text{V}$, $I_T = 4.5\text{mA}$		70	100		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$, unless otherwise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15\text{V}$							
	$I_{SINK} = 10\text{ mA}$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50\text{ mA}$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100\text{ mA}$		2	2.2		2	2.5	V
	$I_{SINK} = 200\text{ mA}$		2.5			2.5		V
	$V_{CC} = 5\text{V}$							
Output Voltage Drop (High)	$I_{SOURCE} = 200\text{ mA}$, $V_{CC} = 15\text{V}$		12.5			12.5		V
	$I_{SOURCE} = 100\text{ mA}$, $V_{CC} = 15\text{V}$	13	13.3		12.75	13.3		V
	$V_{CC} = 5\text{V}$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 164°C/W (TO-5), 106°C/W (DIP), 170°C/W (SO-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at $V_{CC} = 5\text{V}$.

Note 5: Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.

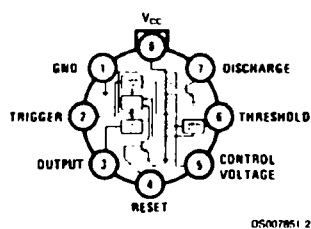
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 M Ω .

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RET555X drawing of military LM555H and LM555J versions for specifications.

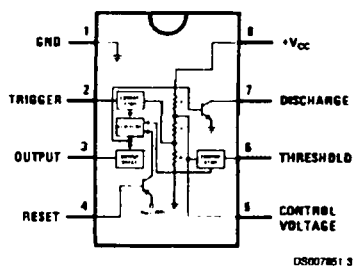
Connection Diagrams

Metal Can Package



Top View
Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View
Order Number LM555J, LM555CJ,
LM555CM, LM555CMM or LM555CN
See NS Package Number J08A, M08A, MUA08A or
N08E

DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin (B) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition ($\overline{\text{L}}$). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations

- Pin-out identical to 'LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity
- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

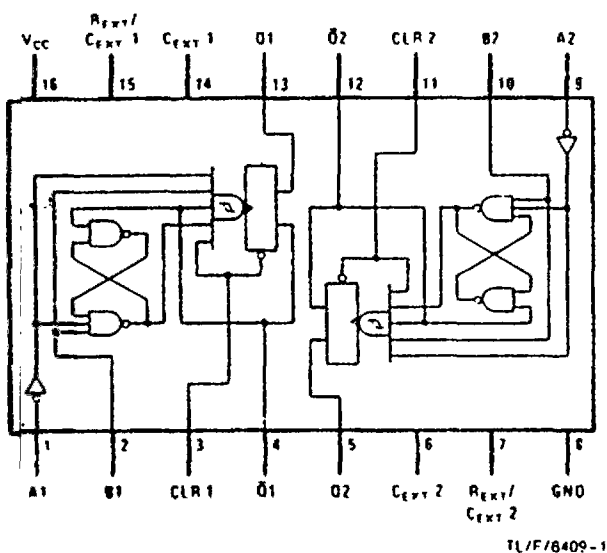
Note 1: The pin-out is identical to 'LS123 but, functionally it is not, refer to Operating Rules # 10 in this datasheet.

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Connection Diagram

Dual-In-Line Package



Order Number DM74LS221M or DM74LS221N
See NS Package Number M16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	\uparrow	$\overline{\text{L}}$	$\overline{\text{H}}$
H	\downarrow	H	$\overline{\text{L}}$	$\overline{\text{H}}$
\uparrow	L	H	$\overline{\text{L}}$	$\overline{\text{H}}$

H = High Logic Level

L = Low Logic Level

X = Can Be Either Low or High

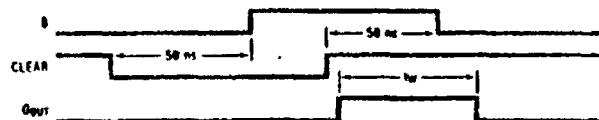
\uparrow = Positive Going Transition

\downarrow = Negative Going Transition

$\overline{\text{L}}$ = A Positive Pulse

$\overline{\text{H}}$ = A Negative Pulse

*This mode of triggering requires first the B input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.



TL/F/8409-2

7400, LS00, S00 Gates

Quad Two-Input NAND Gate
Product Specification

Logic Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7400N, N74LS00N, N74S00N
Plastic SO	N74LS00D, N74S00D

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

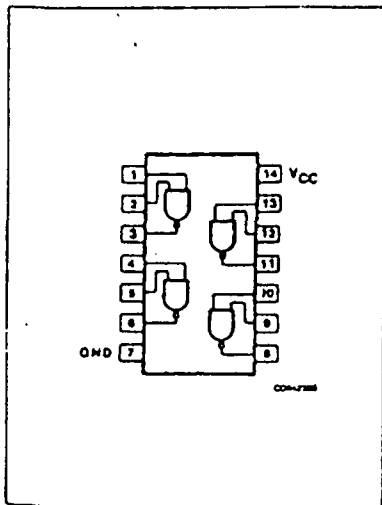
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
A, B	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

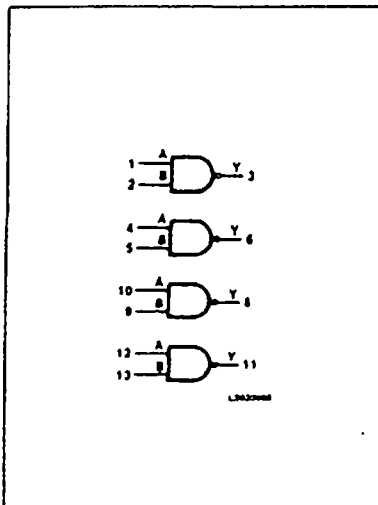
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

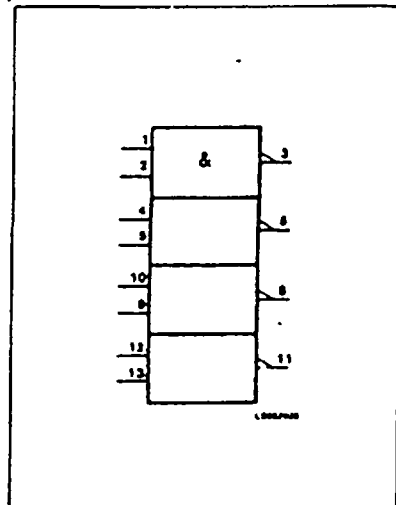
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



54/7446A • 54/7447A
54LS/74LS47
 BCD TO 7-SEGMENT DECODER/DRIVER

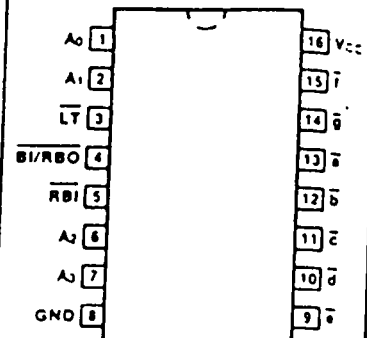
DESCRIPTION — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250 μ A. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression functions. Also see the 'LS247 data sheet.

- OPEN-COLLECTOR OUTPUTS
- DRIVE INDICATOR SEGMENTS DIRECTLY
- CASCADABLE ZERO-SUPPRESSION CAPABILITY
- LAMP TEST INPUT

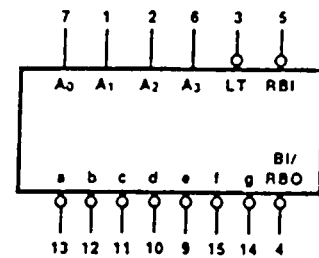
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V \pm 5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V \pm 10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7446APC, 7447APC 74LS47PC		9B
Ceramic DIP (D)	A	7446ADC, 7447ADC 74LS47DC	5446ADM, 5447ADM 54LS47DM	7B
Flatpak (F)	A	7446AFC, 7447AFC 74LS47FC	5446AFM, 5447AFM 54LS47FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
A ₀ — A ₃	BCD Inputs	1.0/1.0	0.5/0.25
RBI	Ripple Blanking Input (Active LOW)	1.0/1.0	0.5/0.25
LT	Lamp Test Input (Active LOW)	1.0/1.0	0.5/0.25
BI/RBO	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)	-/2.5 5.0/5.0	-/0.75 1.25/2.0
a — g	Segment Outputs (Active LOW)	OC*/25	(1.0) OC*/15 (7.5)

*OC — Open Collector

7475, LS75 Latches

Quad Bistable Latch
Product Specification

Logic Products

FEATURES

- 4-bit bistable latch.
- Refer to 74LS375 for V_{CC} and GND on corner pins

DESCRIPTION

The '75 has four bistable latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the O output. The O outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7475	18ns ($t_{p_{LH}}$) 9ns ($t_{p_{HL}}$)	32mA
74LS75	15ns ($t_{p_{LH}}$) 9ns ($t_{p_{HL}}$)	6.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7475N, 1174LS75N
Plastic SO	N74LS25D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual

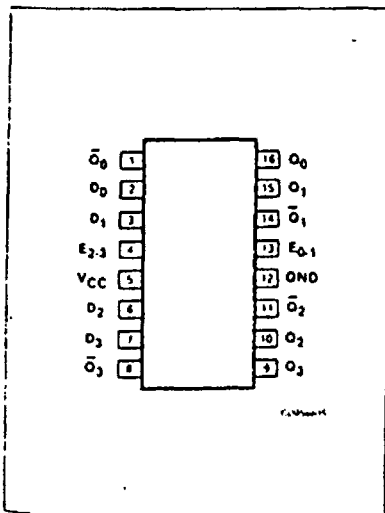
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
D	Input	2uI	1LSuI
E	Input	4uI	4LSuI
All	Outputs	10uI	10LSuI

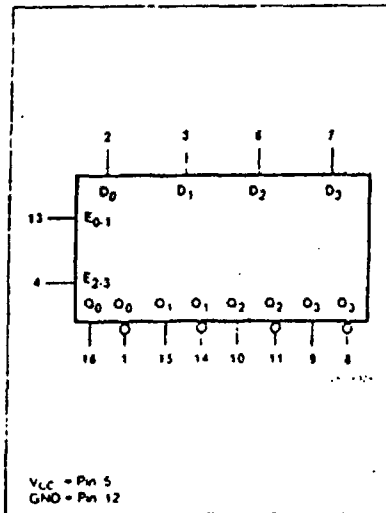
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A I_L$ and $-1.6mA I_H$, and a 74LS unit load (LSuI) is $20\mu A I_L$ and $-0.4mA I_H$.

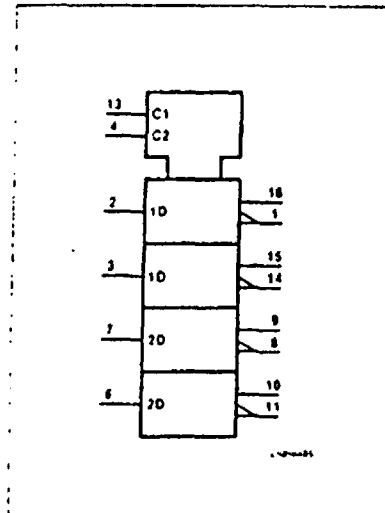
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



7490, LS90 Counters

Decade Counter
Product Specification

Logic Products

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set (MS_1, MS_2) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the \overline{CP}_1 input must be externally connected to the O_0 output. The \overline{CP}_0 input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7490N, N74LS90N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
\overline{CP}_0	Input	2ul	6LSul
\overline{CP}_1	Input	4ul	8LSul
MR, MS	Inputs		1ul
$Q_0 - Q_3$	Outputs	10ul	10LSul

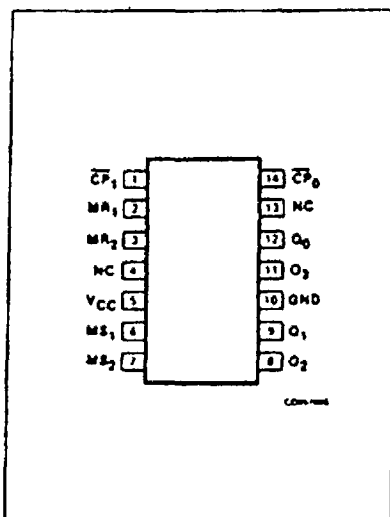
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{HI}$ and $-1.6mA I_{LI}$, and a 74LS unit load (LSul) is $20\mu A I_{HI}$ and $-0.4mA I_{LI}$.

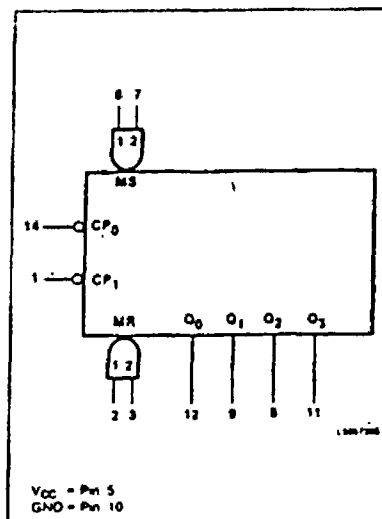
counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the \overline{CP}_1 input and a divide-by-ten square wave is obtained at output O_0 . To operate as a divide-by-two and a divide-by-five count-

er no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function (\overline{CP}_0 as the input and O_0 as the output). The \overline{CP}_1 input is used to obtain a divide-by-five operation at the O_3 output.

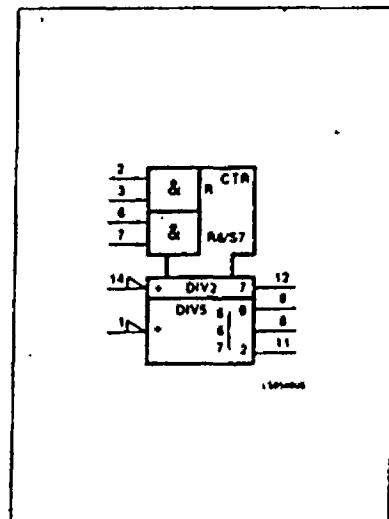
PIN CONFIGURATION



LOGIC SYMBOL



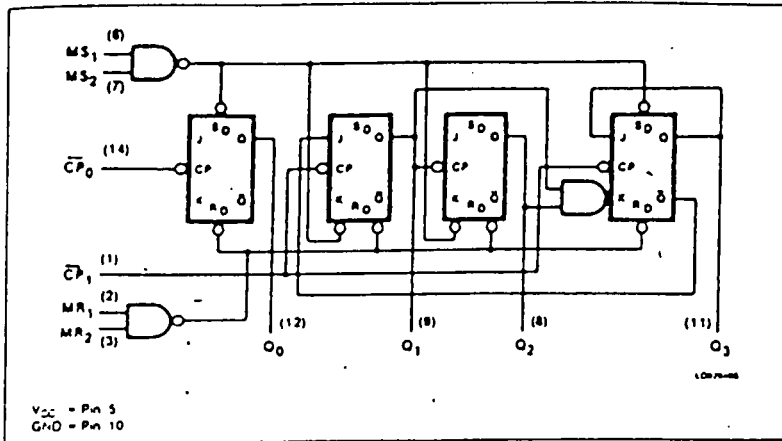
LOGIC SYMBOL (IEEE/IEC)



Counters

7490, LS90

LOGIC DIAGRAM



V_{CC} = Pin 5
GND = Pin 10

MODE SELECTION —
FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
H	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE —
FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE:
Output Q₀ connected to input CP₁

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted)

PARAMETER	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70		°C

NOTE:
V_{IN} is limited to +5.5V on CP₀ and CP₁ inputs on the 74LS90 only.

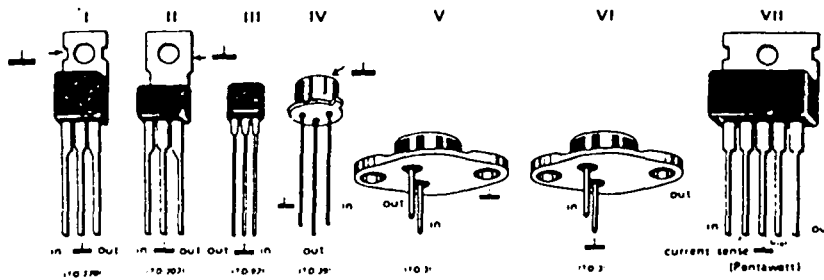
RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V
V _{IL} LOW-level input voltage			+0.8			+0.8	V
I _{IK} Input clamp current			-12			-18	mA
I _{OH} HIGH-level output current			-800			-400	μA
I _{OL} LOW-level output current			16			8	mA
T _A Operating free-air temperature	0		70	0		70	°C

3. Data Regulator Tegangan Positif

tipe part	tegangan keluaran U_o								tegangan masukan maksimum		arus keluaran maksimum A	arus stasioner maksimum mA	rumah	$R_{thj} - a$ lumrah K/W	$R_{thj} - mb$ lumrah K/W
	5 V	6 V	8 V	10 V	12 V	15 V	18 V	24 V	for $U_A = 18 V$ 5 V	for $U_A = 24 V$ 5 V					
78	X	X	X	X	X	X	X	X	35	40	1	42	I	82	3
78M	X	X	X	X	X	X	X	X	35	40	0.5	3	II	79	10
78L	X	X	X	X	X	X	X	X	35	40	0.1	3	III, IV	160/40	-20
LM 309K	X	X	X	X	X	X	X	X	35	40	1	5.2	V	40	3.5
LM 323	X	X	X	X	X	X	X	X	20	35	3	1.2	V	40	3.5
LM 340K	X	X	X	X	X	X	X	X	35	40	1.5	4.2	V	40	3.5
LM 317K	1 2 37 dapat distel								40	40	1.5	0.05	VI	40	3.5
L 200	2 85 36 dapat distel								40	40	2	4.2	VII	50	3

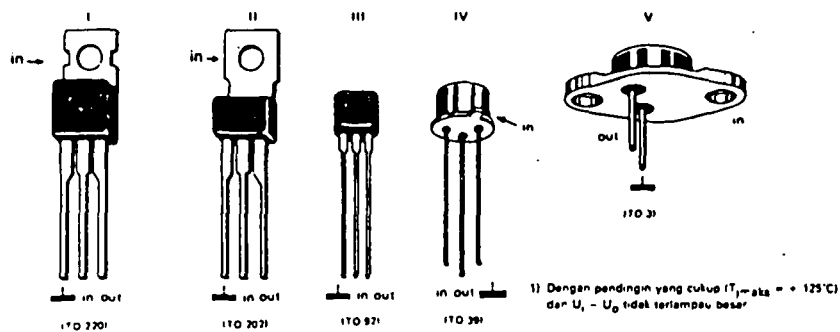
Supaya tegangan keluarannya stabil, tegangan masukan perlu paling kecil 3 kali besar dari tegangan keluaran yang dikehendaki. II with sufficient cooling, $T_{max} = +125^{\circ}C$ and $U_i - U_o$ not too large



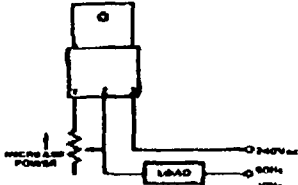
Data Regulator Tegangan Negatif

tipe part	tegangan keluaran U_o								tegangan masukan maksimum		arus keluaran maksimum A	arus stasioner maksimum mA	rumah	$R_{thj} - a$ lumrah K/W	$R_{thj} - mb$ lumrah K/W
	-5 V	-6 V	-8 V	-10 V	-12 V	-15 V	-18 V	-24 V	when $U_o = -5, -18 V$ 5 V	when $U_o = -24 V$ 5 V					
79	X	X	X	X	X	X	X	X	35	40	1	4.2	I	82	3
79M	X	X	X	X	X	X	X	X	35	40	0.5	3	II, IV	79	20
79L	X	X	X	X	X	X	X	X	35	40	0.1	3	III	160/40	-20
LM 345	X	X	X	X	X	X	X	X	20	35	3	1	V	40	3.5
LM 320K	X	X	X	X	X	X	X	X	35	40	1.5	2	V	40	3.5
LM 337K	-1 2 -37 dapat distel								40	40	1.5	0.05	V	40	3.5

Supaya tegangan keluarannya stabil, tegangan masukan perlu lebih negatif dari tegangan keluaran



Discrete Phase Control Regulators



Supplied to **RS** by United Automation Ltd.

Solid state, phase controlled, a.c. mains power regulators which together with an external potentiometer, value 220 k or 250 k linear, will control the power into a load from approx. 0 to 98% (resistive load). Supplied in a convenient-to-mount transistor type housing with integral isolated heat sink tab. Ideal for lamp dimming, heating controls, etc. Suitable heat sinks for full load current at T_{amb} 35°C.

6 A=7°C/W; 8 A=4°C/W; 15 A=2°C/W. To reduce r.f. interference adequate filtering should be incorporated (refer to the Suppressors/Filters section). Connect contact suppressor 238-463 between pins 2 and 3 if snubber network required.

Note: Ensure these devices are mounted to an adequate heat sink. The use of heat sink compound 554-311 is recommended.

Technical Specification

V_{RRM} (tab=70°) 400 V
 I_{Tmax} 6 A, 10 A, 15 A
 I_{TSM} 100 A, 120 A, 150 A
 Min. load current 30 mA
 Hysteresis typ. 5%
 Controlled conduction angle 0-155°
 Tab temp. range -40° to +75°C
 Isolation on tab 1500 V for 1 min.
 Dimensions L. 29.1 (ex. pins) W. 16
 Mounting hole dia. 3.6

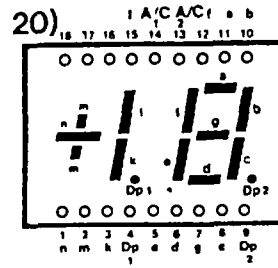
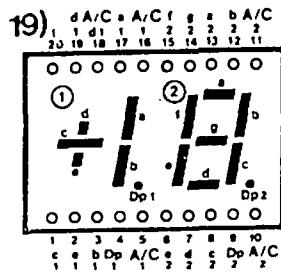
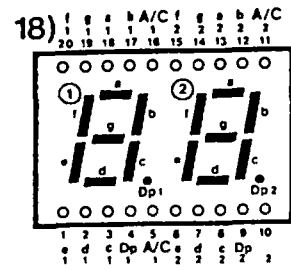
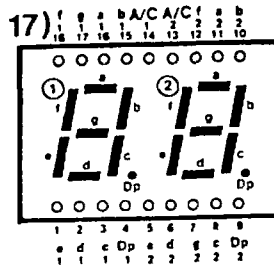
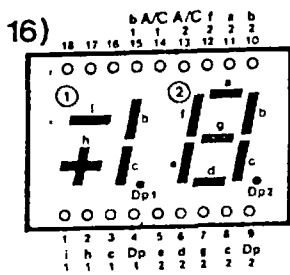
SSM = 1

type stock no.

6 A 300-344
10 A 307-957
15 A 308-584

8. Penampil LED Tujuh-segmen Berdua

tipe	kode warna				kode untuk tunggal		tinggi digit	+10	-10	00	titik dasar		rumah
	merah	kuning	hijau	jingga	anoda	katoda					kiri	kanan	
COX ...	86 .	92 .	90 .	88 .	.. A	.. K	13	X	X	-	X	16	
COX ...	87 .	93 .	91 .	89 .	.. A	.. K	13	-	X	-	X	17	
HA 214 f	-	- 0	... 2 4 .	14	-	X	-	X	18	
HA 214 f	-	- 0	... 3 7 .	14	X	-	-	X	19	
MAN ...	67 ..	-	-	66 10	.. 40	14	-	X	-	X	17	
MAN	67 ..	-	-	66 30	.. 50	14	X	-	-	X	20	



USULAN TUGAS AKHIR

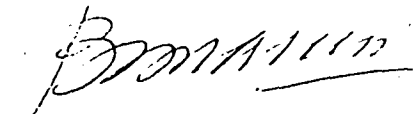
Dosen Pembimbing : Ir. Bunawi Gunawidjaja
Nama Mahasiswa : Leny Poernomo
Bidang Studi : Sistem Tenaga
NIRM Mahasiswa : 92.7.002.31071.01343
NRP Mahasiswa : 23492060
Judul Tugas Akhir : PERENCANAAN DAN PEMBUATAN SOFT STARTER
METODE VARIABEL FREKUENSI MOTOR 220 V
1 PHASE 3/4 HP 2950 RPM 50 HZ.

Lampiran Usulan Tugas Akhir, meliputi :

1. Latar belakang pemilihan judul
2. Ruang lingkup pembahasan
3. Tujuan / sasaran
4. Metode yang digunakan
5. Mata kuliah penunjang
6. Uraian Singkat
7. Jadwal Kegiatan
8. Relevansi

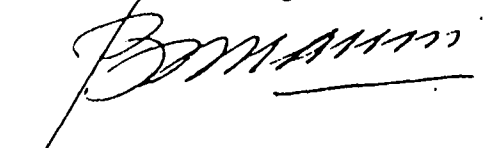
Surabaya, 22 Juni 1997

Mengetahui,
Kepala Bidang Studi



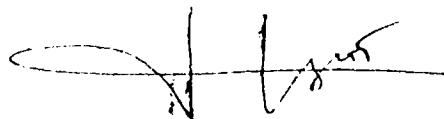
Ir. Bunawi Gunawidjaja

Dosen Pembimbing



Ir. Bunawi Gunawidjaja

Ketua Jurusan



Ir. Hanny H. Tumbelaka M.Sc

PERENCANAAN DAN PEMBUATAN SOFT STARTER METODE VARIABEL FREKUBNSI UNTUK MOTOR 220 V 1 PHASE 3/4 HP 2950 RPM 50 HZ

LATAR BELAKANG PEMILIHAN JUDUL

Perkembangan tenaga listrik pada masa sekarang sangat pesat kemajuannya. Hal ini seiring dengan bertumbuhnya industri-industri yang membutuhkan kehadiran sumber tenaga listrik sebagai penopang kegiatan industrinya. Kebutuhan akan banyaknya energi yang dibutuhkan dari tenaga listrik tersebut, bergantung pada banyaknya motor-motor penggerak yang diperlukan oleh suatu industri.

Banyaknya motor-motor penggerak tersebut akan mempengaruhi arus kerja yang dibutuhkan dari sumber listrik, jika semua motor berjalan secara serempak maka arus kerja yang dibutuhkan juga akan semakin besar. Selain itu perlu juga diperhatikan fungsi, macam, serta karakteristik dari motor penggerak. Hal-hal diatas akan mempengaruhi besarnya permintaan daya/energi listrik yang dibutuhkan dari PLN.

Hal lain yang perlu menjadi pertimbangan adalah arus start/permulaan dari motor saat pertama kali motor dioperasikan. Semakin besar daya dari suatu motor maka akan semakin besar pula arus start yang dibutuhkan. Besar arus start dari motor bisa mencapai 3-6 kali lipat besarnya dari arus nominal/kerja. Jika permintaan sumber energi listrik/daya listrik kepada PLN berdasarkan arus start, maka hal ini tentulah tidak ekonomis serta pada keadaan tertentu akan membuat umur dari motor tidak awet/tahan lama. Diperlukan peralatan yang dapat diaplikasikan pada motor, agar arus start yang tinggi tersebut dapat dikurangi secara drastis. Salah satunya adalah soft starter, alat ini digunakan untuk menjaga arus yang mengalir ke motor pada saat start pertama kali dapat

smooth (tidak terjadi lonjakan arus), sehingga pengaman motor tidak trip karena settingnya pada arus nominal.

RUANG LINGKUP PEMBAHASAN

Pembahasan pada perencanaan dan pembuatan soft starter untuk motor 220 Volt 1 phase dengan metode variabel frekuensi .

TUJUAN / SASARAN

Memberikan pemahaman perencanaan dan pembuatan soft starter untuk motor 220 Volt 1 phase dengan metode variabel frekuensi serta memperlihatkan perbedaan antara frekuensi input dan frekuensi output yang menuju ke motor secara digital

METODE YANG DIGUNAKAN

1. Studi Literatur
2. Perencanaan dan Pembuatan Alat
3. Pengujian Alat
4. Pengumpulan Data
5. Kesimpulan
6. Pembuatan Laporan

MATA KULIAH PENUNJANG

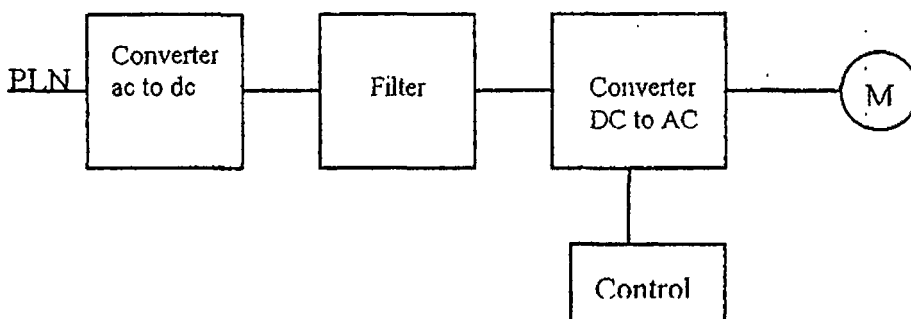
1. Mesin-Mesin Listrik
2. Transformator dan Pemutus

3. Elektronika daya
4. Peralatan Pusat Tenaga listrik I & II
5. Pengukuran Listrik

URAIAN SINGKAT

Soft Starter merupakan suatu alat yang digunakan untuk membantu motor pada saat start. Pada saat start dimana rotor daripada motor akan mulai berputar sesuai dengan putaran spesifikasi motor tersebut, maka diperlukan arus yang sangat besar dibanding dengan arus nominal/kerja. Dengan adanya soft start variabel frekuensi, diharapkan rotor akan berputar secara bertahap dari putaran yang rendah hingga putaran nominalnya. Hal ini bisa dilakukan dengan cara memberikan supply tegangan dengan frekuensi yang mula-mula rendah hingga tercapai frekuensi 50 Hz pada motor. Sehingga arus yang diperlukan dari sistem tidak melonjak beberapa kali lipat dari arus nominal motor tersebut. Diharapkan dengan soft starter maka pemakaian arus/energi listrik dari sistem tidak terganggu saat motor dalam keadaan start.

BLOK DIAGRAM



JADWAL KEGIATAN

Kegiatan	Bulan					
	I	II	III	IV	V	VI
Studi Literatur	XXXX	XXXX				
Perencanaan Alat		XXXX	XXXX			
Pembuatan Alat			XXXX	XXXX		
Pengujian Alat					XXXX	
Pengumpulan Data					XXXX	
Kesimpulan					XXXX	
Pembuatan Naskah					XXXX	XXXX

RELEVANSI

Soft starter banyak digunakan di industri-industri untuk menjaga lonjakan arus (besarnya bisa mencapai beberapa kali lipat dari arus nominal) pada saat motor distart/diopcrasikan. Sehingga sistem tenaga listrik tidak mengalami gangguan saat motor akan diopcrasikan.